Production of a hall bar

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Abstract

The *Student Cleanroom* experiment's goal is to produce a hall bar in three main steps. Students etch the mesa, add ohmic contacts and adhere a top gate. Figure 6 shows the final result. The resistance of two opposing annealed contacts connected by the 2DEG is 1.7 kΩ to 2.2 kΩ at room temperature.

1 Introduction

The intention of the educational laboratory course *Praktikum 3* is for students to gain experience with experimental physics. This includes preparatory research, hands-on work using modern tools and techniques, analysing measurements and describing process and results in a scientifically written report.

This specific experiment *Student Cleanroom* introduces students to two dimensional electronic systems[6]. They produce a hall bar, a micro scale device which can be used as a transistor, using optical lithography. As this experiment also serves as a practical introduction to solid state physics and the experimenters are third year undergraduates and either have not or are in the process of hearing lectures on the topic, many aspects such as a precise description of the samples composition as well as manufacturing techniques and the underlying theory go beyond the scope of this experiment and the experimenters current understanding. However, resources such as the provided outtakes from Stephen A. Campbell's *Fabrication Engineering at the Micro and Nanoscale*[1] for lithography and Motoi Takahashi's doctoral thesis *Transport Characteristics in GaAs/AlGaAs Quantum Structures*[8] for fabrication provide a deeper insight and have been proven very helpful.

2 Method

The process consists of fabricating the hall bar and subsequent measuring of its properties. Figure 1 outlines the three main steps of fabrication.

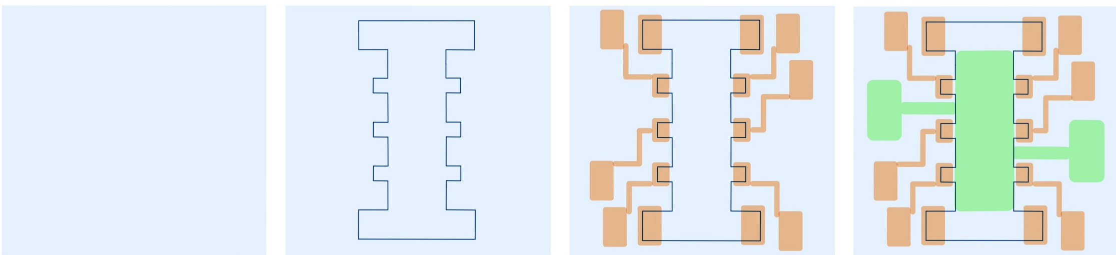

Figure 1: From left to right: starting from a clean, cleaved (subsection 2.1) sample, subsequent etching the mesa of the hall bar, creating ohmic contacts and finally adding a top gate the experimenters manufacture a micro scale transistor called hall bar.

2.1 The GaAs/AlGaAs sample

The sample is a rectangular chip approximately on the order of a square centimetre in area. The original wafer simplified consists of a gallium arsenide (GaAs) substrate, a layer of aluminium gallium arsenide (AlGaAs) and GaAs heterostructure forming the conductive two-dimensional-electron-gas (2DEG) in the middle and a layer of GaAs on top. Since GaAs is of a zincblende structure, splitting the round wafer into chips with a diamond cleaver leaves vertical borders[2].

2.2 Preparation and Precautions

In order to protect themselves and the sample, experimenters take a number of precautions. A cleanroom creates a pressure gradient from sample to experimenter reducing contamination. Additional physical barriers such as Plexiglas windows, suits, surgical masks, gloves, as well as a box filled with gel protect the sample. As some processes are sensitive to short wavelength light, UV-blocking foil covers the windows. Protective glasses and aforementioned clothing also protect experimenters from potentially dangerous chemicals.

Various outside sources contaminate the sample during production, transportation and storage. If not specified otherwise, "cleaning the sample" refers to the process of inserting the chip in an ultrasonic cleaning device, 1-3 minutes in a bath of acetone which removes particles and 1-2 minutes in a bath of isopropanol which removes the acetone, at 50°C and 10% of the cleaners maximum capacity, depending on the degree of pollution. Ultrasonic cleaners increase the effectiveness of the solvents by inducing compression cycles which create bubbles, whose implosions release force which in turn dislodges contaminants[7]. Instead of air drying, blowing off acetone with a nitrogen spray gun leaves a cleaner sample.

2.3 Etching the mesa - positive photolithography

Restricting current onto desired areas requires shaping the 2DEG. A hall bar's mesa can have many shapes, in this experiment it is the one sketched in the second subfigure in Figure 1.
After transferring the clean and dry sample (Figure 2, subfigure ⓪) onto a 100 °C hotplate and allowing any liquids to evaporate for 3 minutes a spin coater holds the sample in its center using a vacuum. Then, rotating at 4000 rpm for 15 s ramp-up-time and 50 s of spinning, it applies a 1.8 µm layer of the positive photoresist AZ 1518 [4]①. The *soft bake*, a 60 s placement on the 100 °C hotplate, prepares resist for a 5 s exposure by the mask aligner equipped with a high intensity mercury lamp. For photoresist not covered by a chrome pattern of a photo mask, which has the shape of the mesa, illumination ③ alters its properties ④. All steps outlined in Figure 1 use the same mask, but the sample is placed under different areas of it, such that always the pattern corresponding to the, at this point in process, relevant one of the three steps is transferred. Furthermore, the mask contains the same step design multiple times to ensure optimal placement possibilities. Immersing the pattern in the chemical developer MIF 362 dissolves illuminated parts of the resist ⑤, hence the name *positive* photoresist.

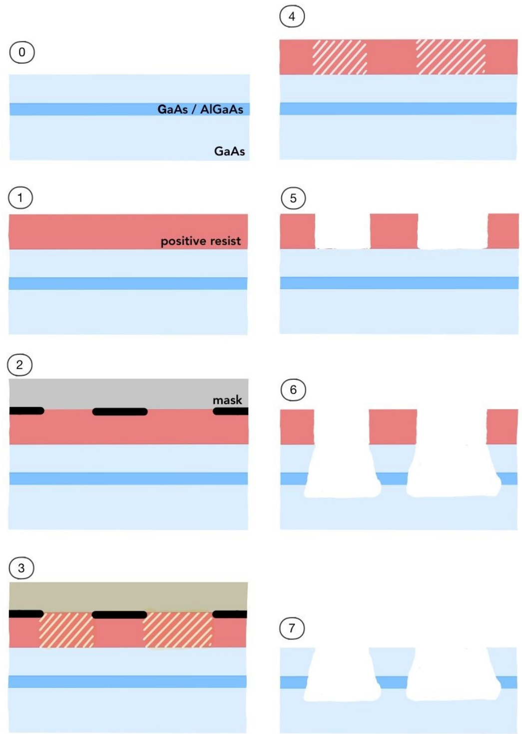

Figure 2: Process of positive photolithography and etching, sketch not to scale

Inserting the sample into an etching chemical composed of 100 parts H_2O, 3 parts H_2SO_4 and 3 parts H_2O_2 for 205 s transfers the resist's pattern into the chip and past the 2DEG, although not anisotropically ⑦.

2.4 Adding ohmic contacts and measuring resistance

Once the 2DEG in the chip has the desired hall bar shape, the second step is adding contacts to the mesa pattern (third image in Figure 1) to enable applying current through the hall bar. Negative photoresist, here AZ nLOF 2020, instead of positive photoresist is better suited for subsequent steps because it creates stronger bonds during exposure and *post exposure bake* in the parts that are not developed away (polymerization/cross-linking), which reduces softening when coating with metals, and during development it can create a slope in the exposed resist called *undercut*, which assists in *liftoff* [3]. Spinning (see Figure 3, subfigure ①) requires the same settings as in subsection 2.3, but soft bake happens at 110 °C at still 60 s. To align the mask pattern of the contacts with the mesa ②, special alignment squares have been placed in both the mesa and the contacts pattern during mask design.

A 2 s exposure in the mask aligner ③ and an immediate transfer to a 110 °C hotplate for 120 s called *post exposure bake* to alter chemical composition ⑤. As in positive photolithography, MIF 326 develops the mask pattern into the resist for 120 s, but this time adds bit of an undercut ⑥. The assistant then deposits layers of germanium (Ge), gold (Au), nickel (Ni) and gold again (bottom to top) ⑦, all on the order of 10 nm to 100 nm, in a procedure called *electron beam lithography* (EBL). This combination of metals allows for a low contact resistance to the 2DEG once the contacts have been annealed in step ⑨. Beforehand however, metal on resist as well as resist is removed in a process called *liftoff* using the solvent dimethyl sulfoxide (DMSO) ⑧. Then annealing the sample at 600 mbar in N_2H_2 for 120 s at 120 °C followed by 20 s at 450 °C ⑨ eliminates the Schottky barrier, a potential barrier resulting from the energy band bending at the interface between metal and semiconductor[5]. The result is an ohmic contact, which means that current is linear with respect to voltage.

A setup consisting of a multimeter that applies a current to the chip through two needles placed on the contacts (see Figure 4) with a microscope enables measuring the total resistance across the shorter axis of the hall bar. The resistance of a single contact is then approximately half the total resistance since the 2DEG at room temperatures is very conductive and the resistances are in series. Its magnitude corresponds to the slope displayed on the curve tracer (green screen in Figure 4). On the vertical axis it shows voltage drop per applied current and on the horizontal axis total voltage drop. The result follows immediately from Ohm's law $V = R \cdot I$.

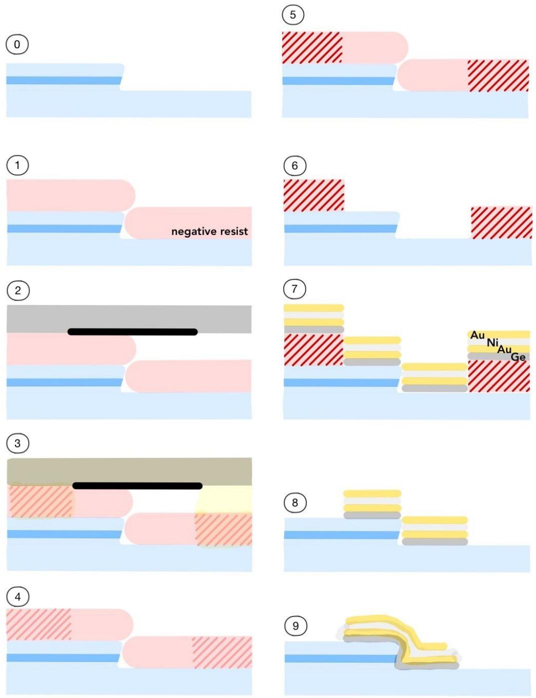

Figure 3: Process of negative photolithography and adding ohmic contacts, sketch not to scale

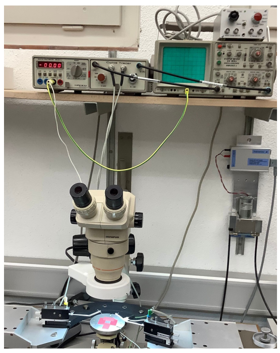

Figure 4: Setup resistance measurement

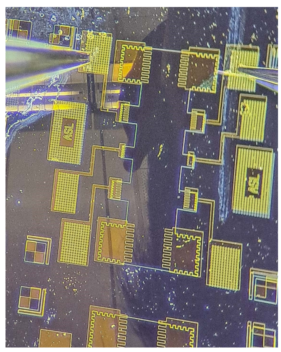

Figure 5: Chip with needles on contacts

2.5 Top gate

What makes the hall bar a transistor is its ability to allow or disallow flow of a current much larger than what is needed for its own operation. Adding a top gate and not removing the Schottky barrier allows for potential modulation without injecting current.

Adding the top gate is a very similar process to the one of adding ohmic contacts. The few exceptions are of course different mask design (see rightmost subfigure in Figure 1), that 3 nm of titanium (Ti) followed by 150 nm of gold are deposited instead of the Ge-Au-Ni-Au combination (where the titanium mainly just adheres the gold to the GaAs) and that, for above mentioned reasons, the gate is not annealed. See section 3 for the final result.

3 Results and discussion

The physical result of the fabrication process is the finished hall bar in Figure 6, which as a device was not quantitatively in this experiment. However, the resistance measurements of the annealed contacts connected by the 2DEG sum up to 1.7 kΩ to 2.2 kΩ at room temperature. Differences of up to 0.5 kΩ are the result of the measurement being sensitive to even small disruptions in the setup.

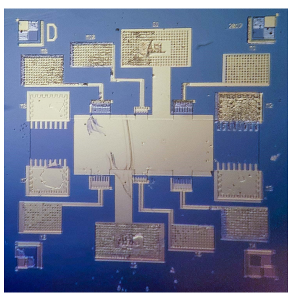

Figure 6: Final hall bar with mesa, ohmic contacts and top gate, aligned by the squares in the corners

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